

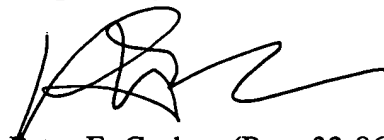
20. The circuit arrangement of claim 16 wherein provision is made of a comparator for comparing the instantaneous write address provided by an address counter with the penultimate writing start address stored, the output of the comparator being connected to a flip-flop for driving a multiplexer, and
in that the penultimate writing start address stored is present at a first input of the multiplexer and the last writing start address stored is present at a second input of the multiplexer, with the result that, in the event of correspondence between the instantaneous write address of the address counter and the penultimate writing start address stored, the multiplexer outputs the last writing start address stored as reading start address, whereas otherwise the multiplexer outputs the penultimate writing start address stored as reading start address.

REMARKS

To reduce initial filing fees, claims 1-10 have been cancelled without prejudice, and claims 11-20 have been added. No new matter has been added by virtue of the new claims. For instance, support for the new claims appears e.g. in the original claims of the application.

Early consideration and allowance of the application are earnestly solicited.

Respectfully submitted,



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